OIPE JC48
FEB 09 2004
PATENT & TRADEMARK OFFICE

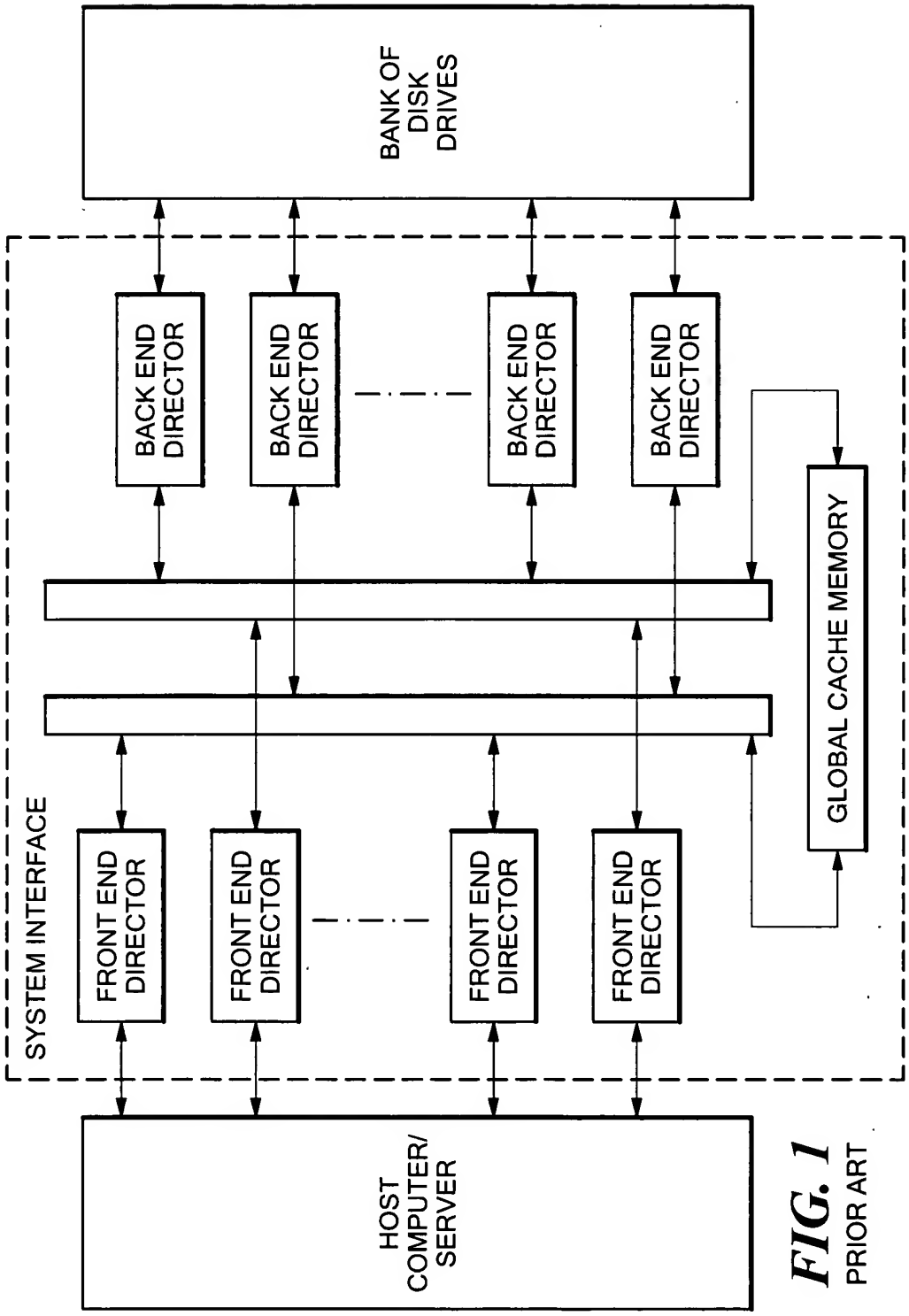

FIG. 1
PRIOR ART

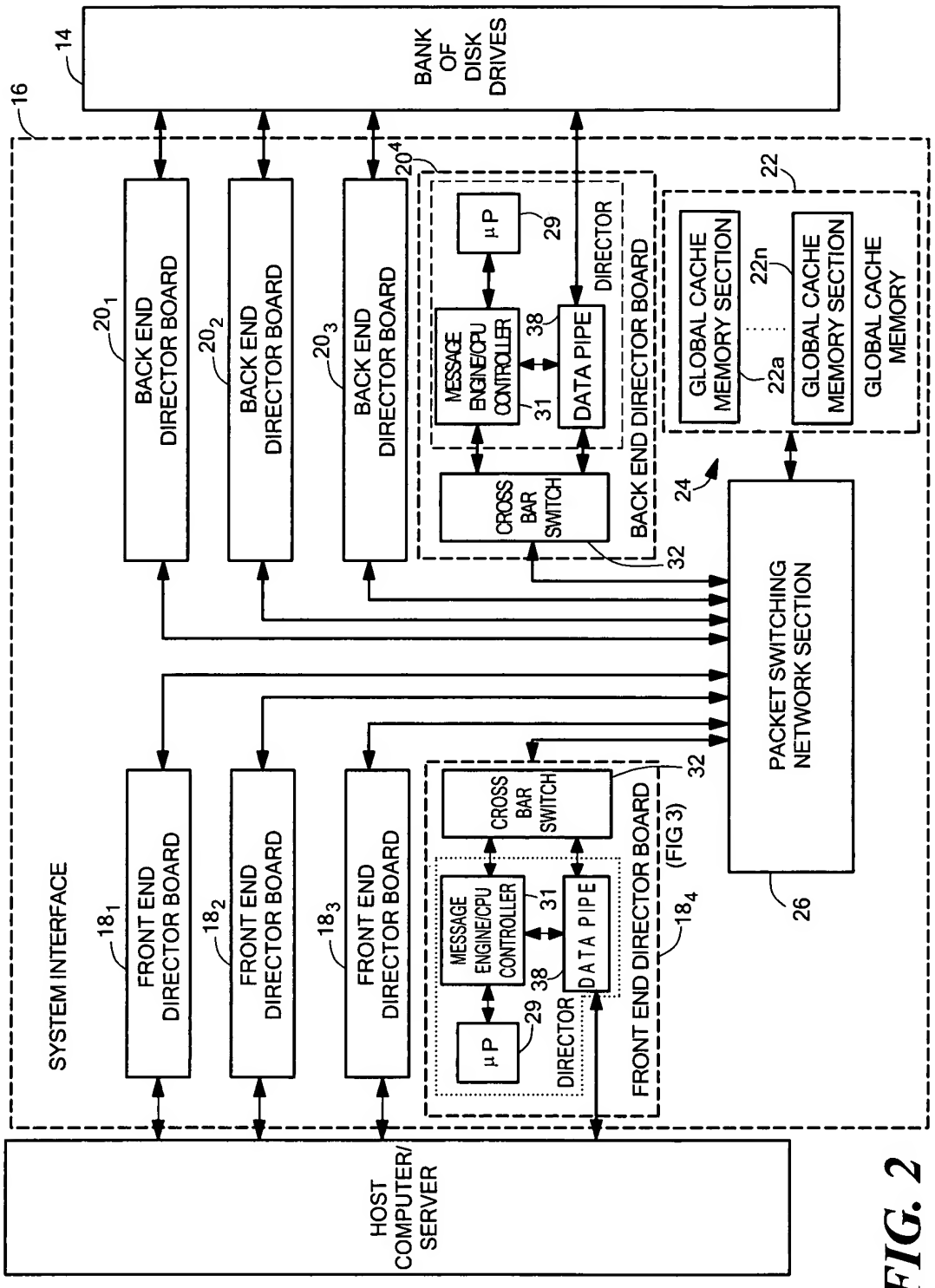
BANK OF DISK DRIVES
14
16
SYSTEM INTERFACE
BACK END DIRECTOR BOARD
20_1
20_2
20_3
20_4
BACK END DIRECTOR BOARD
DIRECTOR
µP
29
MESSAGE ENGINE/CPU CONTROLLER
31
38
DATA PIPE
CROSS BAR SWITCH
32
22
GLOBAL CACHE MEMORY SECTION
22a
22n
GLOBAL CACHE MEMORY
24
PACKET SWITCHING NETWORK SECTION
26
FRONT END DIRECTOR BOARD
18_1
18_2
18_3
18_4
(FIG 3)
HOST COMPUTER/ SERVER

FIG. 2

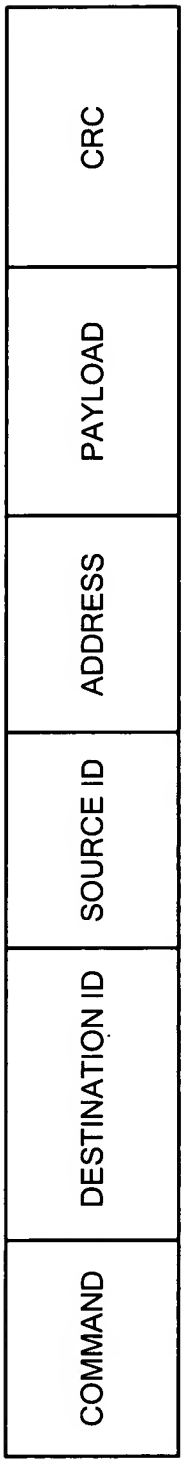
COMMAND
DESTINATION ID
SOURCE ID
ADDRESS
PAYLOAD
CRC

FIG. 2A

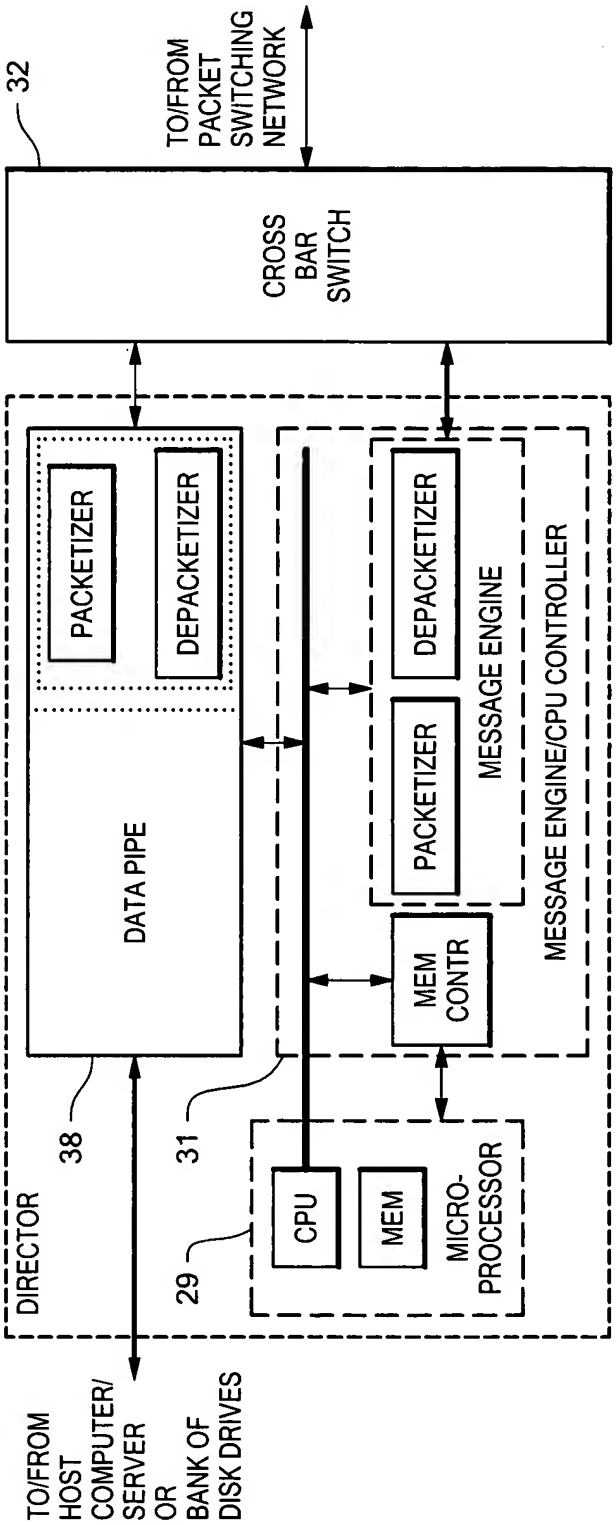
32
TO/FROM PACKET SWITCHING NETWORK
CROSS BAR SWITCH
DIRECTOR
PACKETIZER
DEPACKETIZER
DATA PIPE
38
31
29
DEPACKETIZER
PACKETIZER
MESSAGE ENGINE
MESSAGE ENGINE/CPU CONTROLLER
MEM CONTR
CPU
MEM
MICRO-PROCESSOR
TO/FROM HOST COMPUTER/ SERVER OR BANK OF DISK DRIVES

FIG. 3

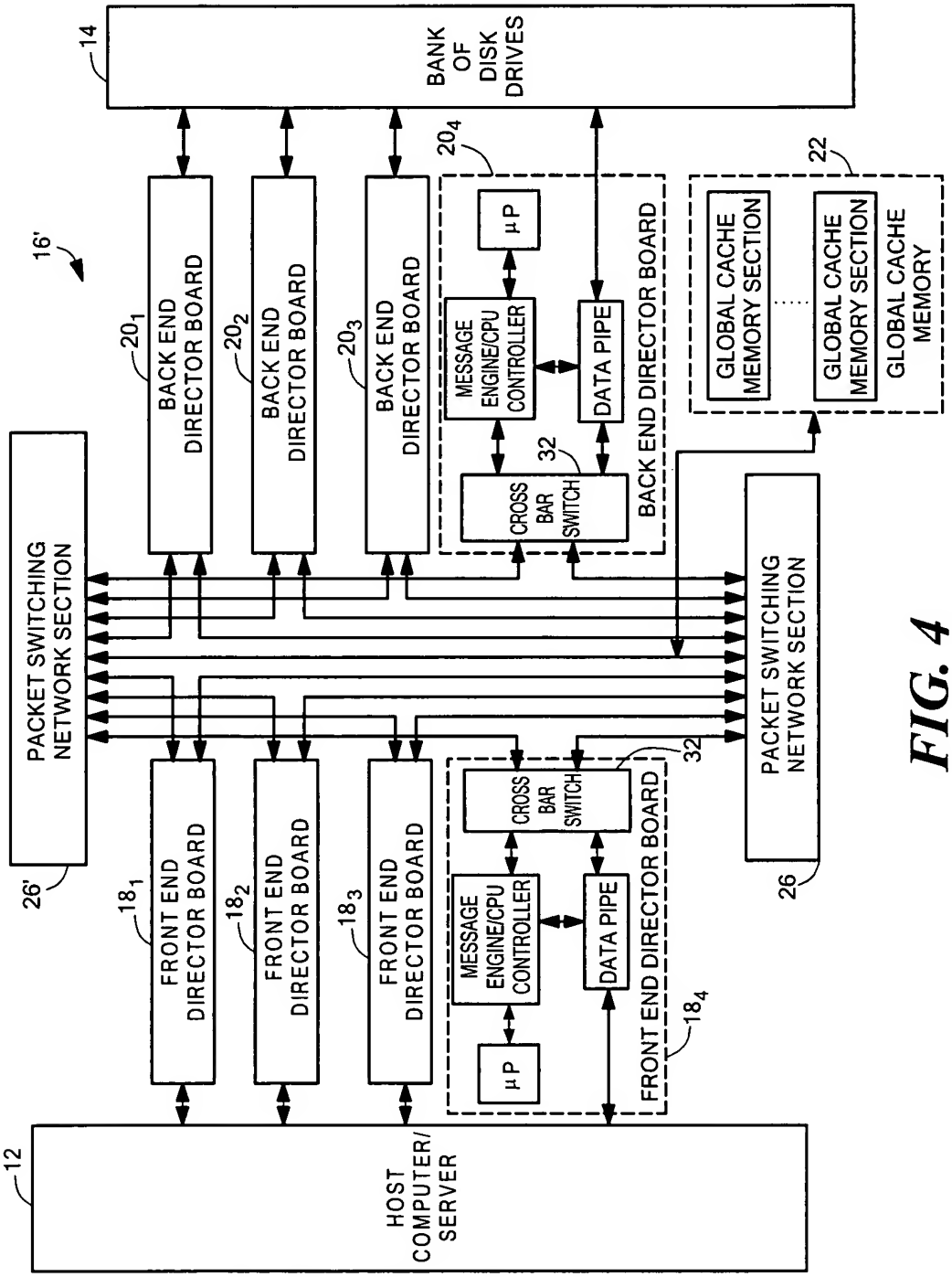
14
BANK OF DISK DRIVES
16'
20$_1$
BACK END DIRECTOR BOARD
20$_2$
BACK END DIRECTOR BOARD
20$_3$
BACK END DIRECTOR BOARD
20$_4$
μP
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
CROSS BAR SWITCH
32
BACK END DIRECTOR BOARD
22
GLOBAL CACHE MEMORY SECTION
GLOBAL CACHE MEMORY SECTION
GLOBAL CACHE MEMORY
PACKET SWITCHING NETWORK SECTION
26'
PACKET SWITCHING NETWORK SECTION
26
18$_1$
FRONT END DIRECTOR BOARD
18$_2$
FRONT END DIRECTOR BOARD
18$_3$
FRONT END DIRECTOR BOARD
CROSS BAR SWITCH
32
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
μP
18$_4$
FRONT END DIRECTOR BOARD
12
HOST COMPUTER/ SERVER

FIG. 4

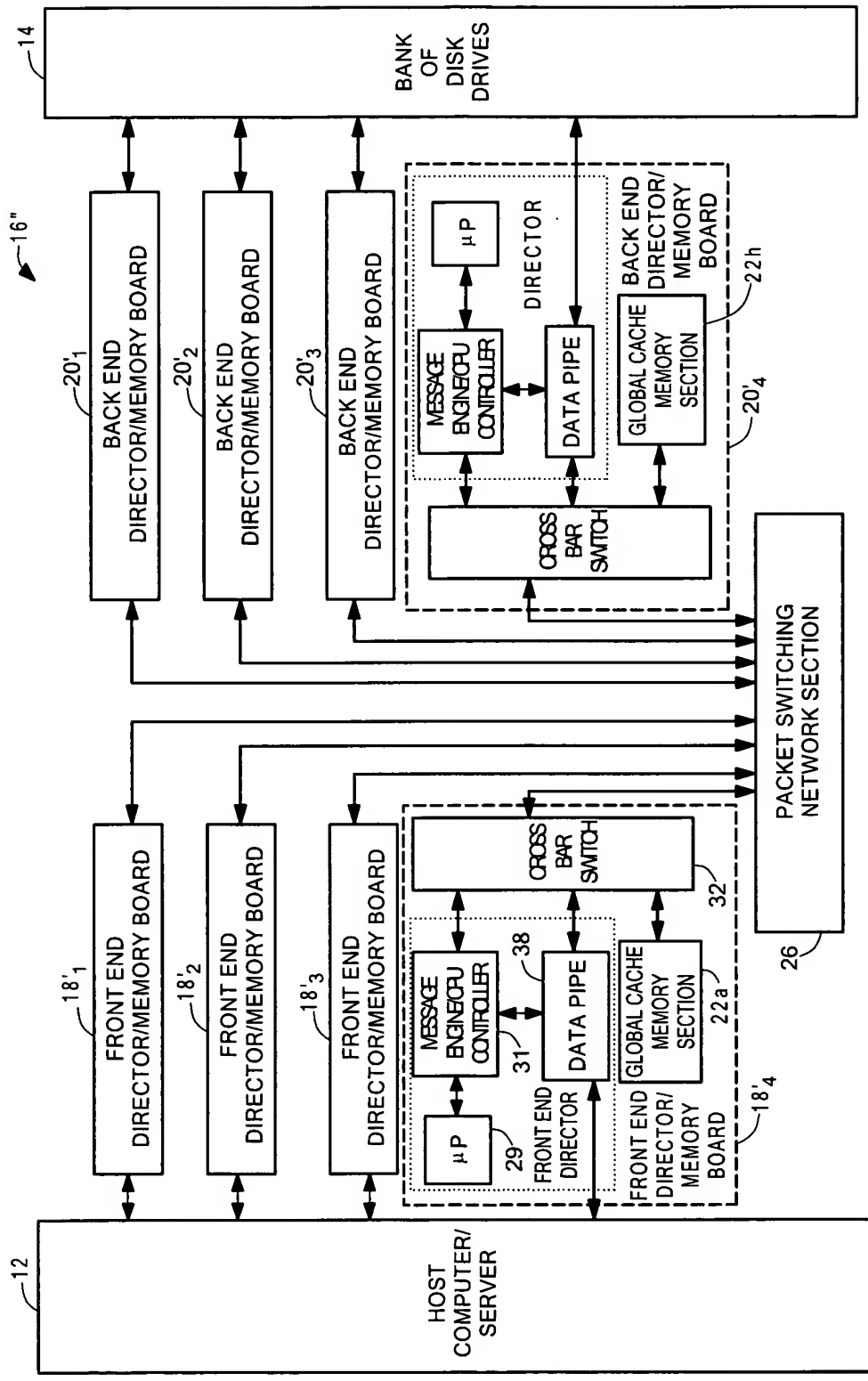
14
BANK OF DISK DRIVES
16"
20'1
BACK END DIRECTOR/MEMORY BOARD
20'2
BACK END DIRECTOR/MEMORY BOARD
20'3
BACK END DIRECTOR/MEMORY BOARD
20'4
BACK END DIRECTOR/MEMORY BOARD
22h
GLOBAL CACHE MEMORY SECTION
DIRECTOR
µP
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
CROSS BAR SWITCH
PACKET SWITCHING NETWORK SECTION
26
18'1
FRONT END DIRECTOR/MEMORY BOARD
18'2
FRONT END DIRECTOR/MEMORY BOARD
18'3
FRONT END DIRECTOR/MEMORY BOARD
18'4
FRONT END DIRECTOR/MEMORY BOARD
32
38
31
22a
29
FRONT END DIRECTOR
12
HOST COMPUTER/SERVER

FIG. 5

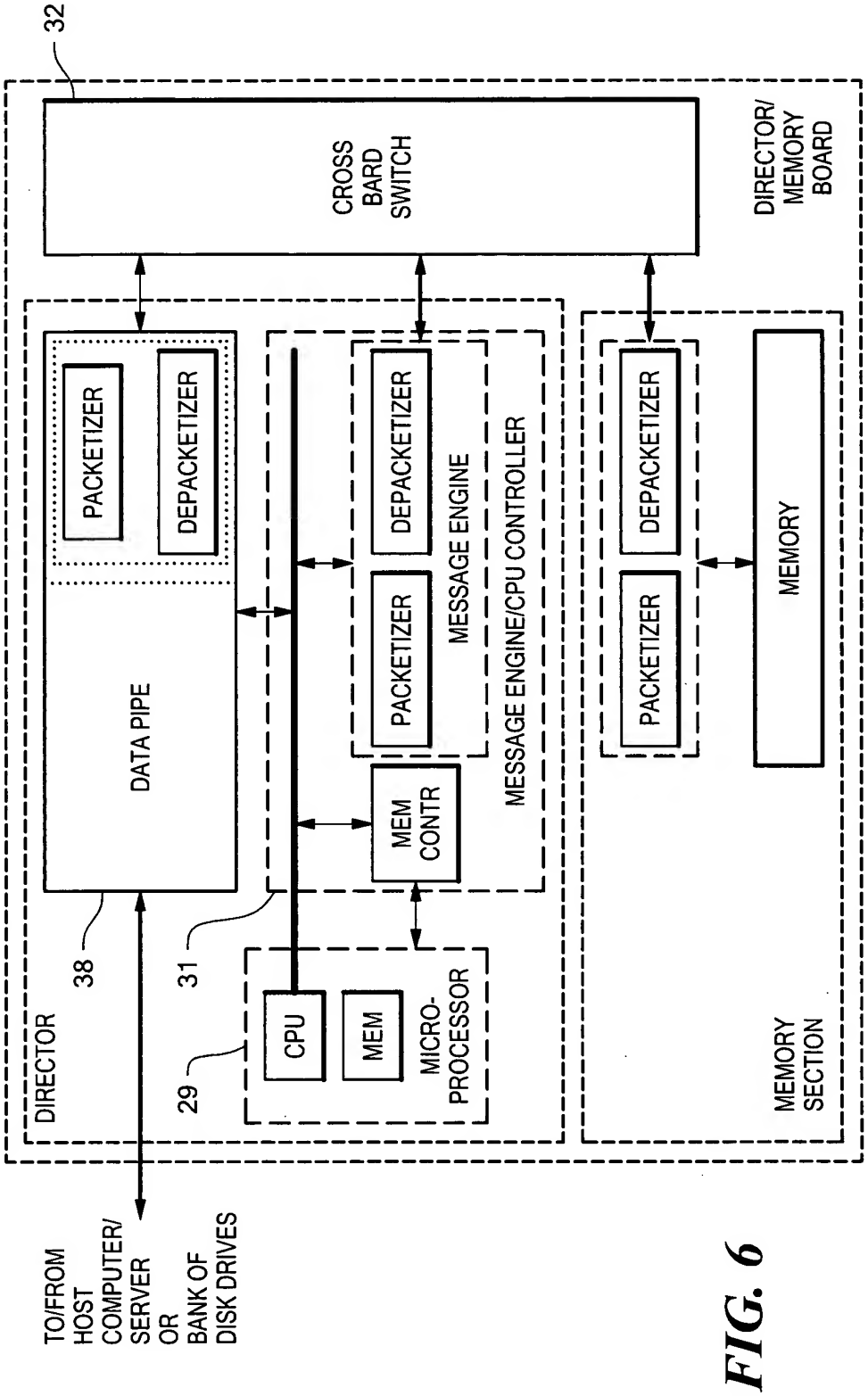
32
CROSS BARD SWITCH
DIRECTOR/ MEMORY BOARD
PACKETIZER
DEPACKETIZER
DATA PIPE
DEPACKETIZER
PACKETIZER
MESSAGE ENGINE
MESSAGE ENGINE/CPU CONTROLLER
MEM CONTR
DEPACKETIZER
PACKETIZER
MEMORY
38
31
29
CPU
MEM
MICRO-PROCESSOR
DIRECTOR
MEMORY SECTION
TO/FROM HOST COMPUTER/ SERVER OR BANK OF DISK DRIVES

FIG. 6

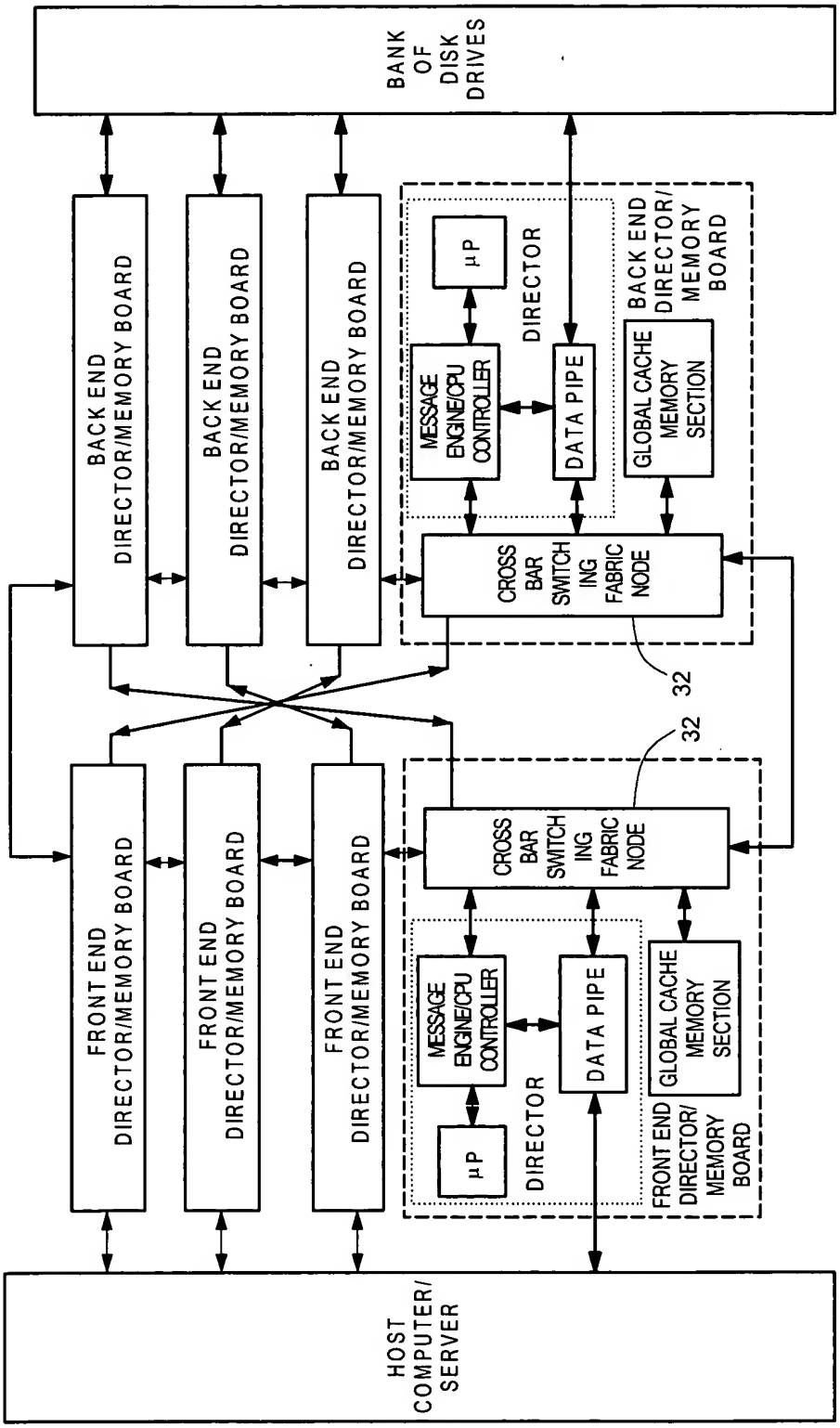
BANK OF DISK DRIVES
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
μP
DIRECTOR
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
BACK END DIRECTOR/ MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
32
32
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
μP
DIRECTOR
FRONT END DIRECTOR/ MEMORY BOARD
HOST COMPUTER/ SERVER

FIG. 7

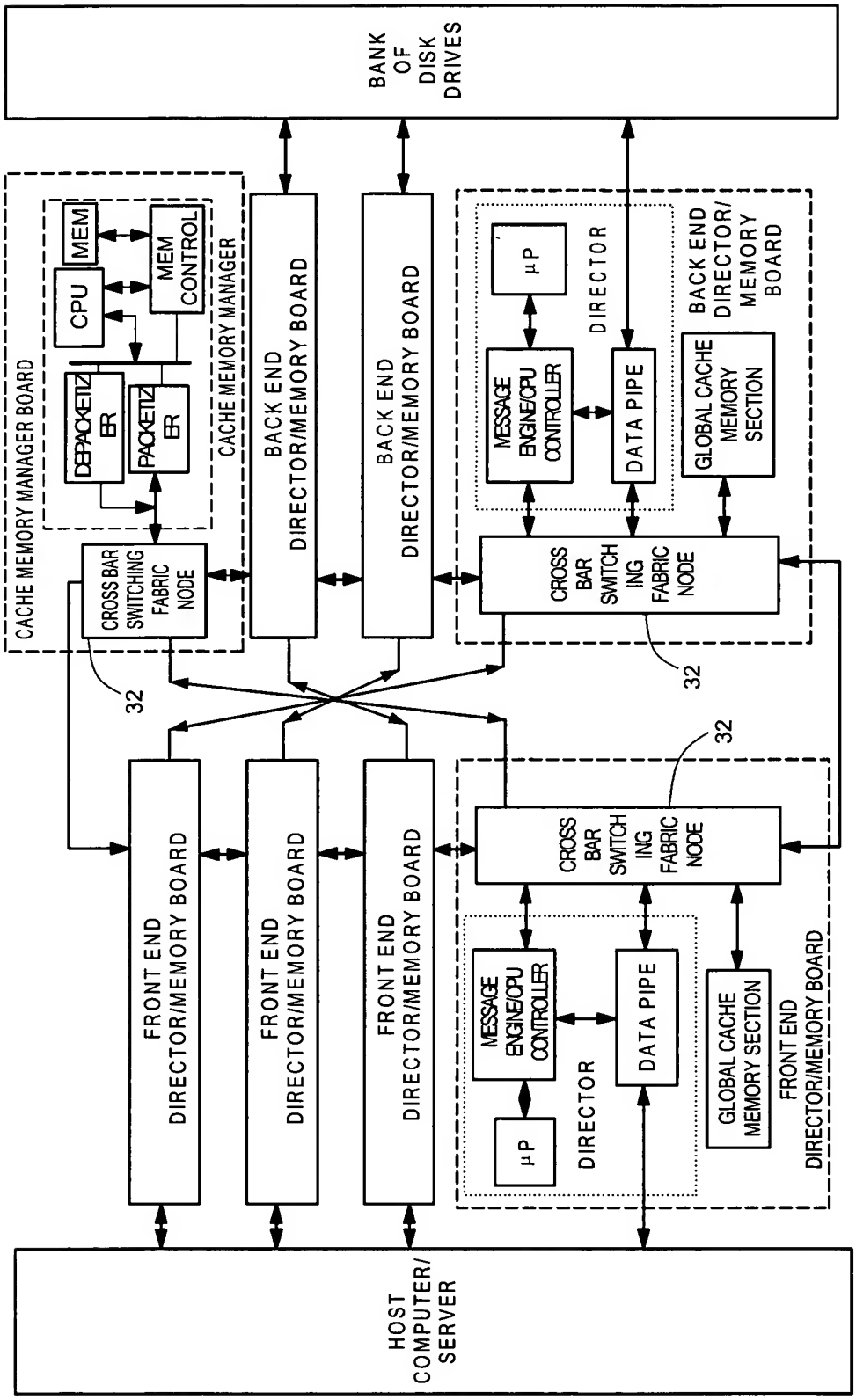
BANK OF DISK DRIVES
CACHE MEMORY MANAGER BOARD
CACHE MEMORY MANAGER
MEM
CPU
MEM CONTROL
DEPACKETIZER
PACKETIZER
CROSS BAR SWITCHING FABRIC NODE
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
DIRECTOR
µP
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
BACK END DIRECTOR/ MEMORY BOARD
CROSS BAR SWITCHING FABRIC NODE
32
32
32
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
CROSS BAR SWITCHING FABRIC NODE
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
µP
DIRECTOR
FRONT END DIRECTOR/MEMORY BOARD
HOST COMPUTER/ SERVER

FIG. 7A

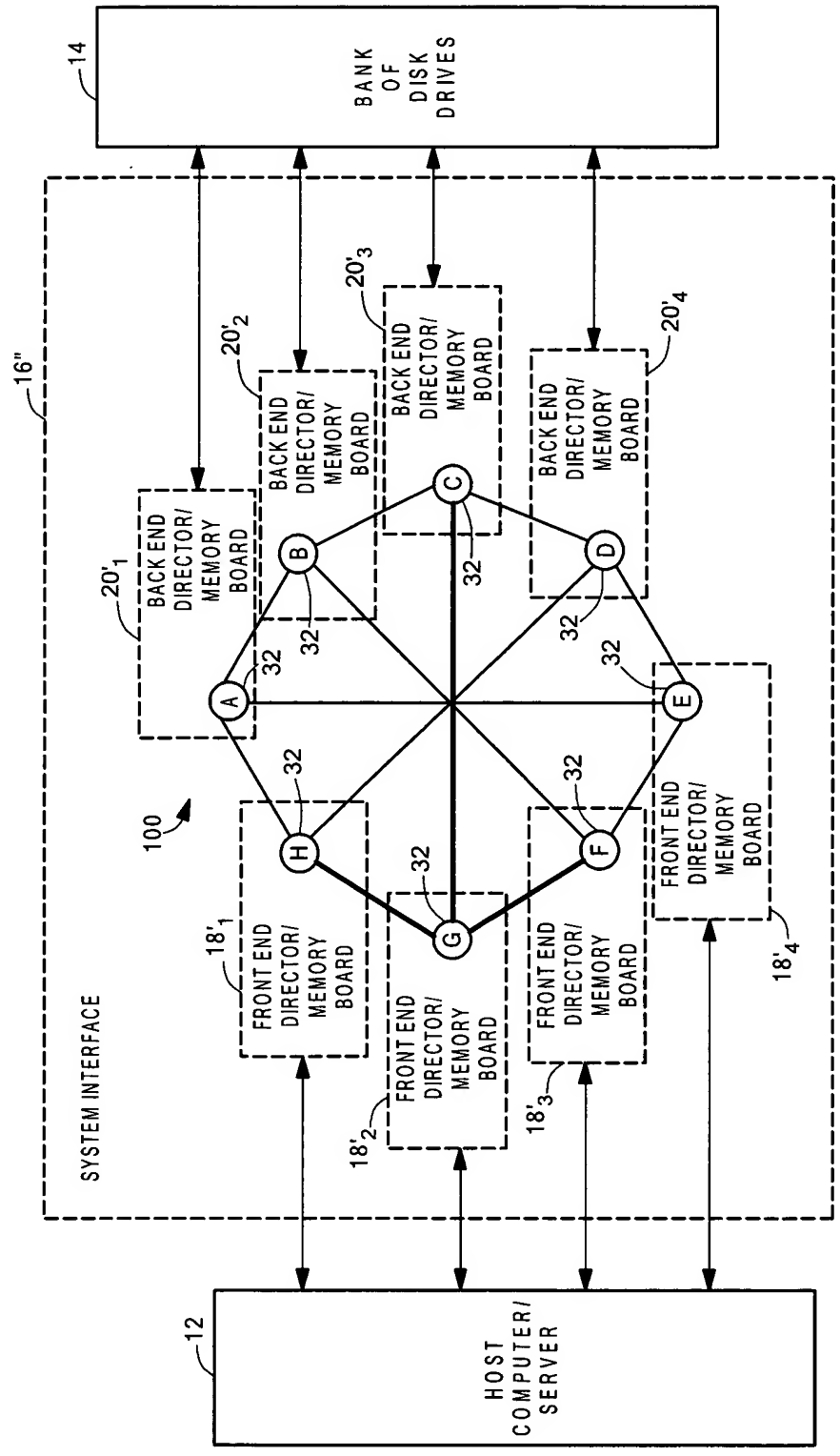
14
BANK OF DISK DRIVES
16"
SYSTEM INTERFACE
20'1
BACK END DIRECTOR/ MEMORY BOARD
20'2
BACK END DIRECTOR/ MEMORY BOARD
20'3
BACK END DIRECTOR/ MEMORY BOARD
20'4
BACK END DIRECTOR/ MEMORY BOARD
18'1
FRONT END DIRECTOR/ MEMORY BOARD
18'2
FRONT END DIRECTOR/ MEMORY BOARD
18'3
FRONT END DIRECTOR/ MEMORY BOARD
18'4
FRONT END DIRECTOR/ MEMORY BOARD
A
B
C
D
E
F
G
H
32
100
12
HOST COMPUTER/ SERVER

FIG. 8

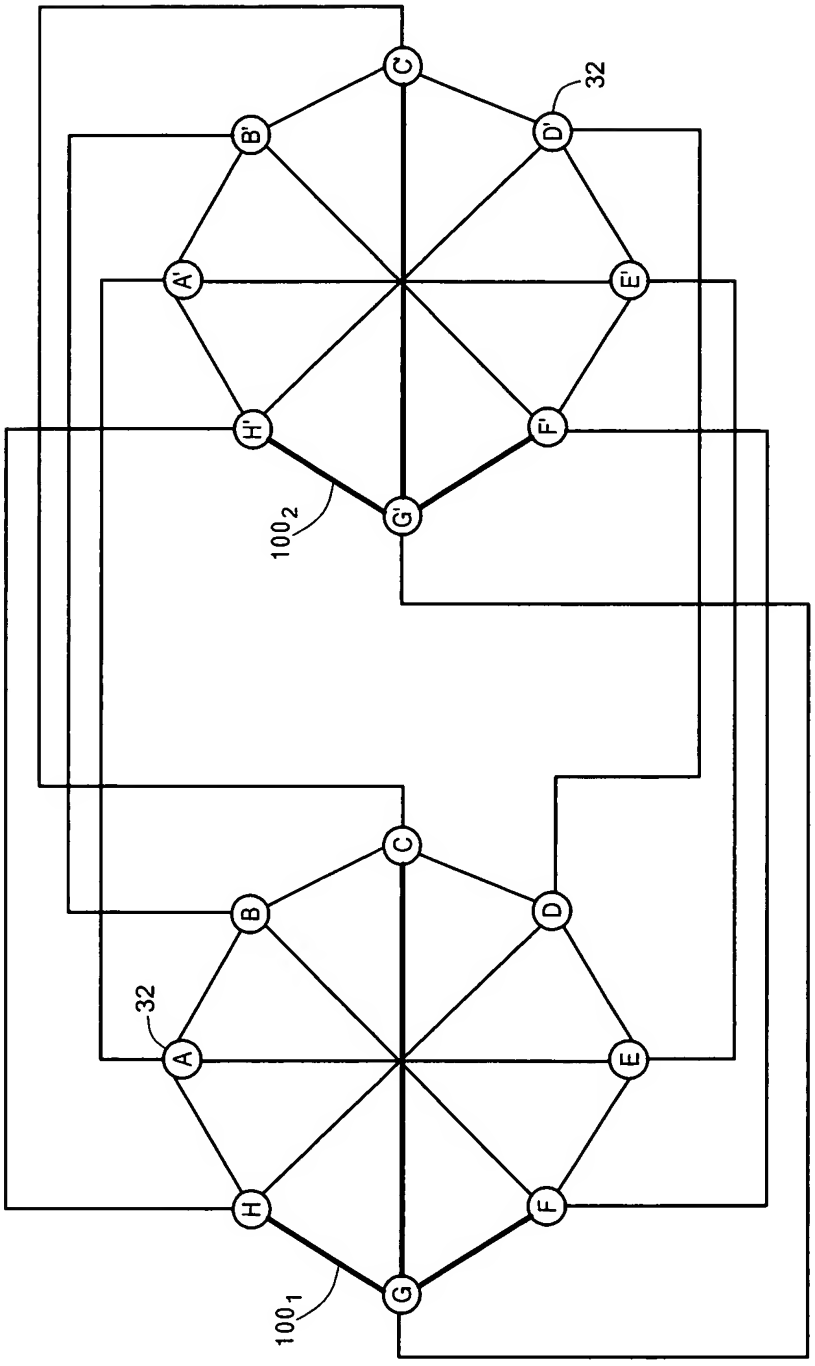

FIG. 9A

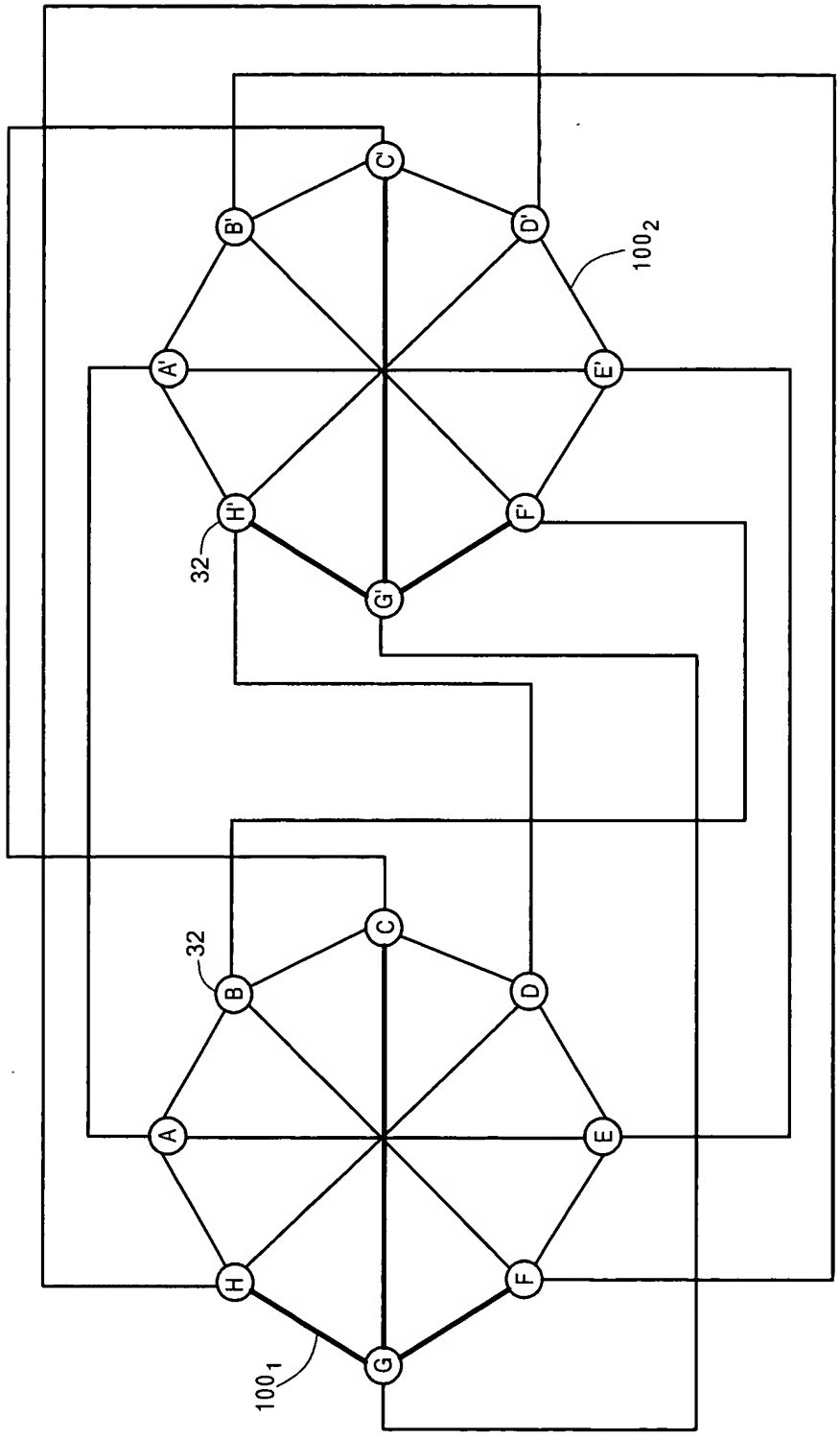

FIG. 9B

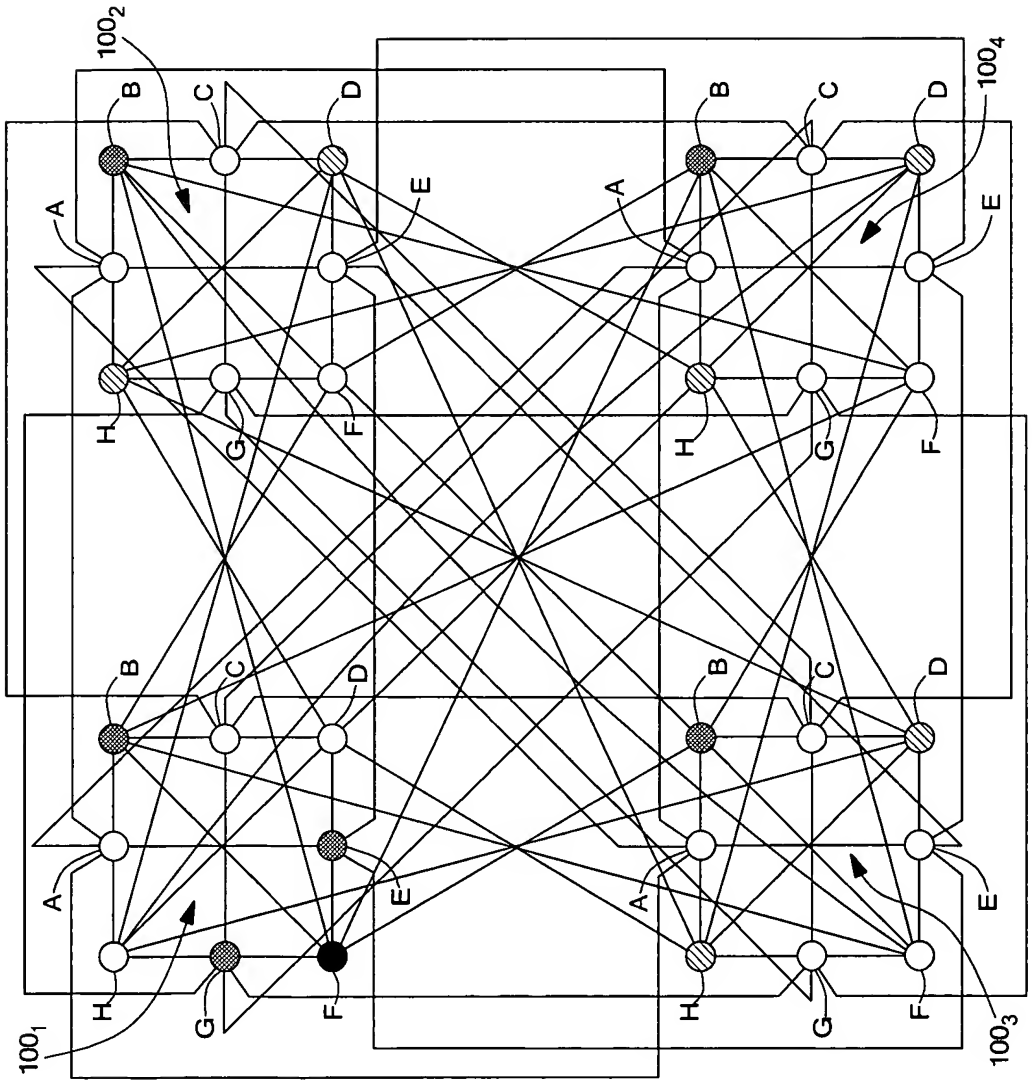
Starting Point. S
Direct Attach
One Switch Delay, "1"
Two Switch Delays, "2"
100_1 - 100_4
A
B
C
D
E
F
G
H
100_1
100_2
100_3
100_4

FIG. 9C

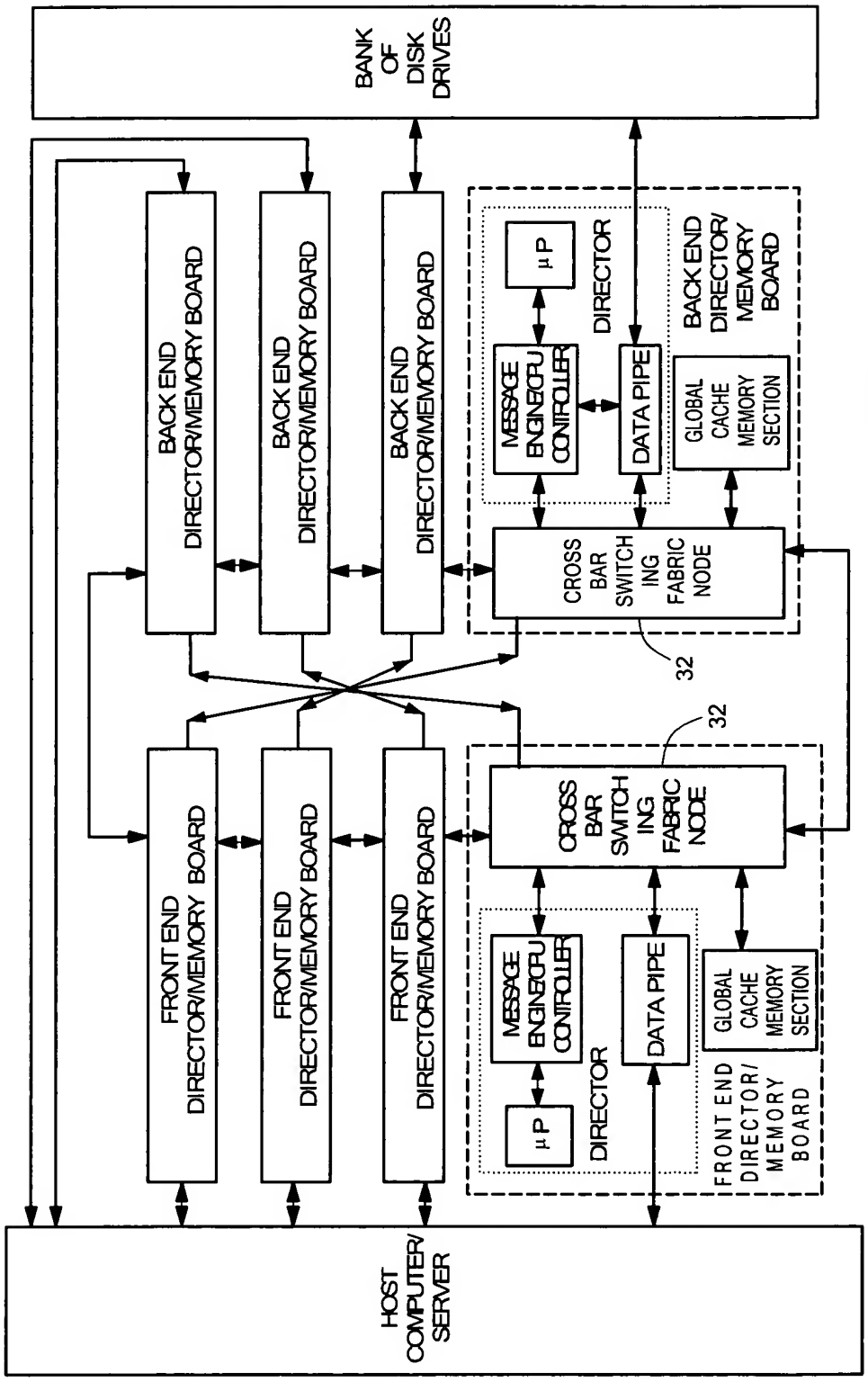
BANK OF DISK DRIVES
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
μP
DIRECTOR
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
BACK END DIRECTOR/ MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
32
32
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
μP
DIRECTOR
FRONT END DIRECTOR/ MEMORY BOARD
HOST COMPUTER/ SERVER

FIG. 10

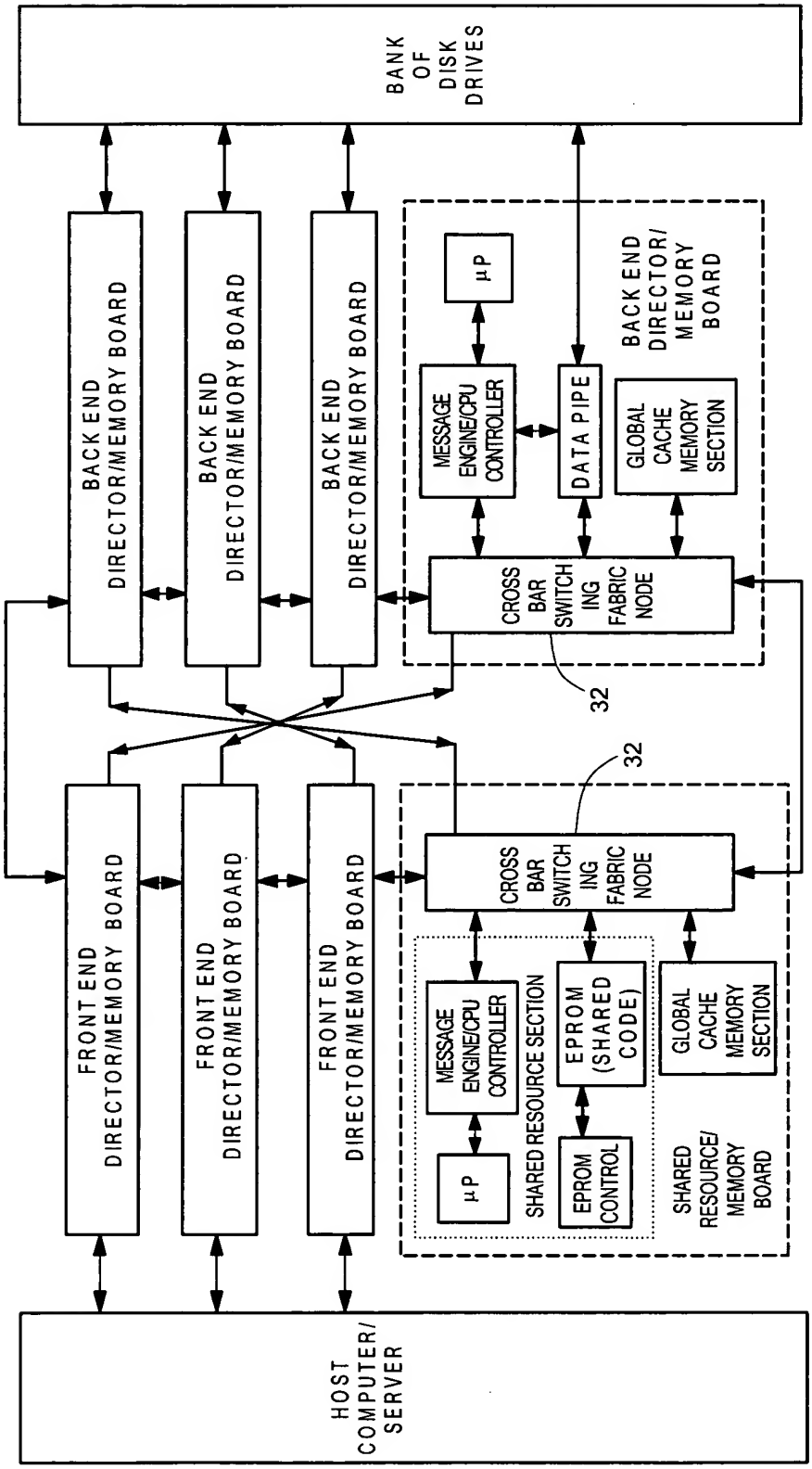
BANK OF DISK DRIVES
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
μP
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
BACK END DIRECTOR/ MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
32
32
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
MESSAGE ENGINE/CPU CONTROLLER
EPROM (SHARED CODE)
GLOBAL CACHE MEMORY SECTION
SHARED RESOURCE SECTION
μP
EPROM CONTROL
SHARED RESOURCE/ MEMORY BOARD
HOST COMPUTER/ SERVER

FIG. 11

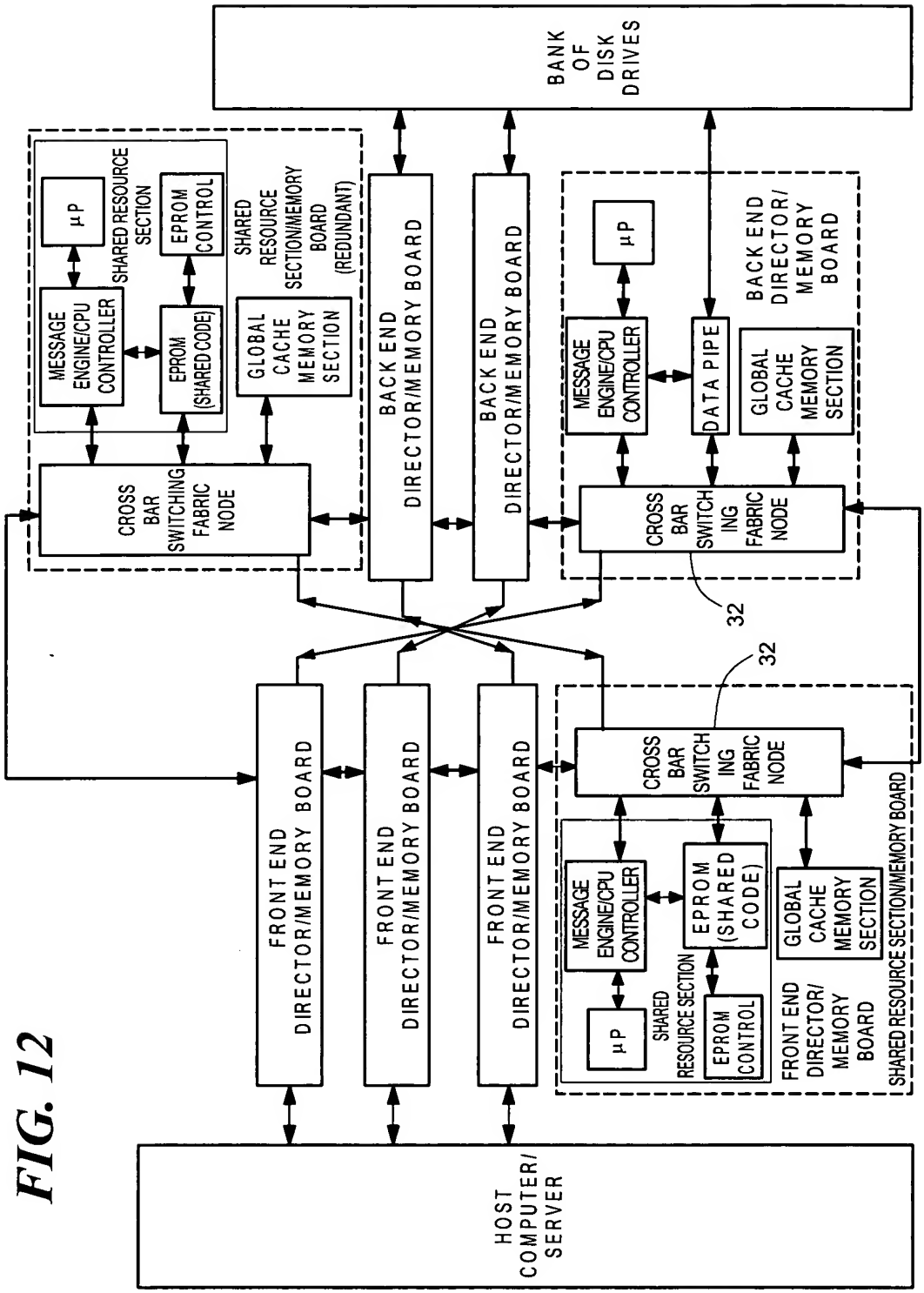
BANK OF DISK DRIVES
SHARED RESOURCE SECTION
µP
EPROM CONTROL
MESSAGE ENGINE/CPU CONTROLLER
EPROM (SHARED CODE)
GLOBAL CACHE MEMORY SECTION
SHARED RESOURCE SECTION/MEMORY BOARD (REDUNDANT)
CROSS BAR SWITCHING FABRIC NODE
BACK END DIRECTOR/MEMORY BOARD
BACK END DIRECTOR/MEMORY BOARD
µP
MESSAGE ENGINE/CPU CONTROLLER
DATA PIPE
GLOBAL CACHE MEMORY SECTION
BACK END DIRECTOR/ MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
32
32
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
FRONT END DIRECTOR/MEMORY BOARD
CROSS BAR SWITCH ING FABRIC NODE
MESSAGE ENGINE/CPU CONTROLLER
EPROM (SHARED CODE)
GLOBAL CACHE MEMORY SECTION
µP
SHARED RESOURCE SECTION
EPROM CONTROL
FRONT END DIRECTOR/ MEMORY BOARD
SHARED RESOURCE SECTION/MEMORY BOARD
HOST COMPUTER/ SERVER

FIG. 12

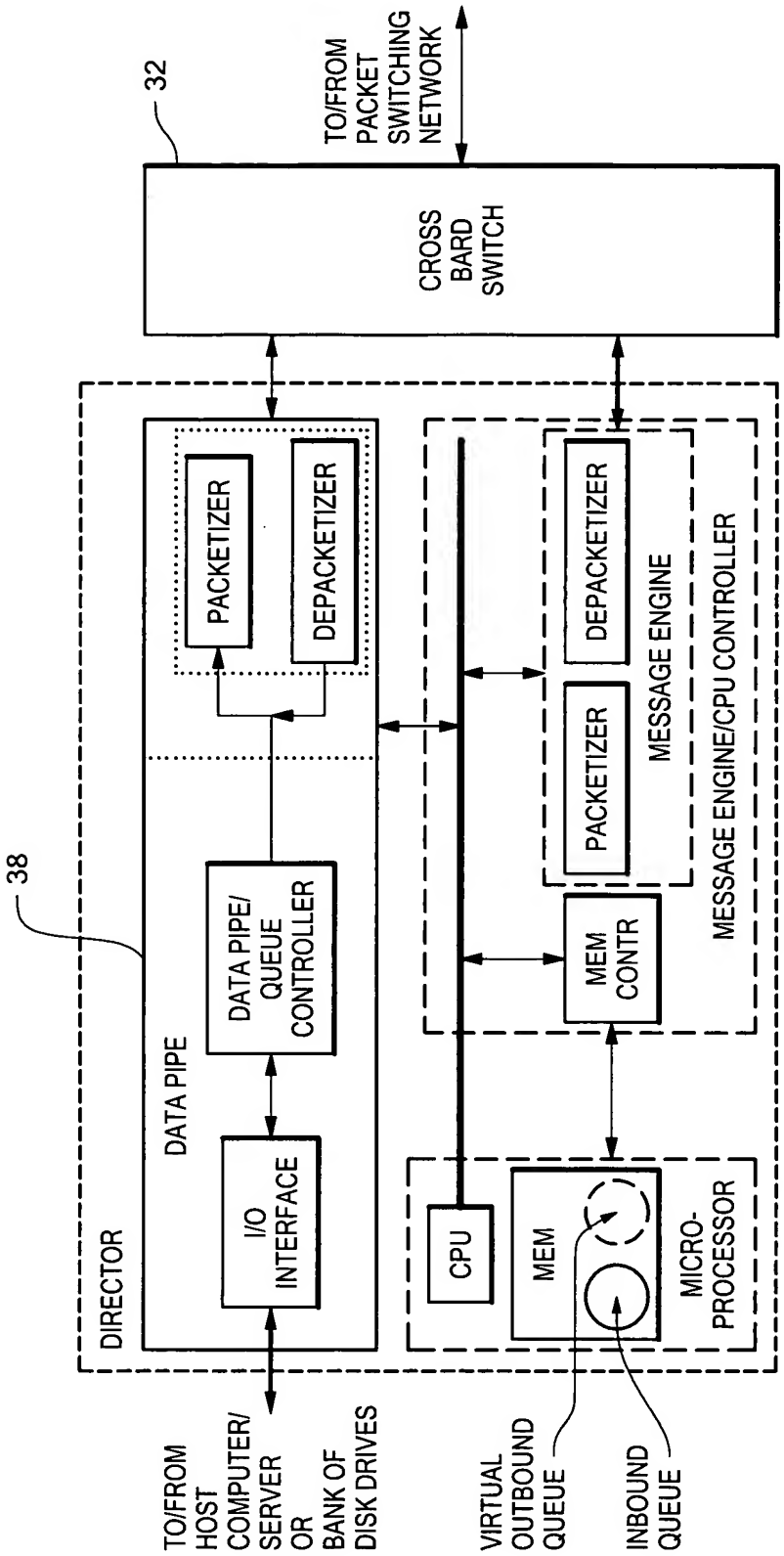
32
TO/FROM PACKET SWITCHING NETWORK
CROSS BARD SWITCH
PACKETIZER
DEPACKETIZER
DEPACKETIZER
PACKETIZER
MESSAGE ENGINE
MESSAGE ENGINE/CPU CONTROLLER
38
DATA PIPE/ QUEUE CONTROLLER
DATA PIPE
MEM CONTR
I/O INTERFACE
CPU
MEM
MICRO-PROCESSOR
DIRECTOR
TO/FROM HOST COMPUTER/ SERVER OR BANK OF DISK DRIVES
VIRTUAL OUTBOUND QUEUE
INBOUND QUEUE

FIG. 13

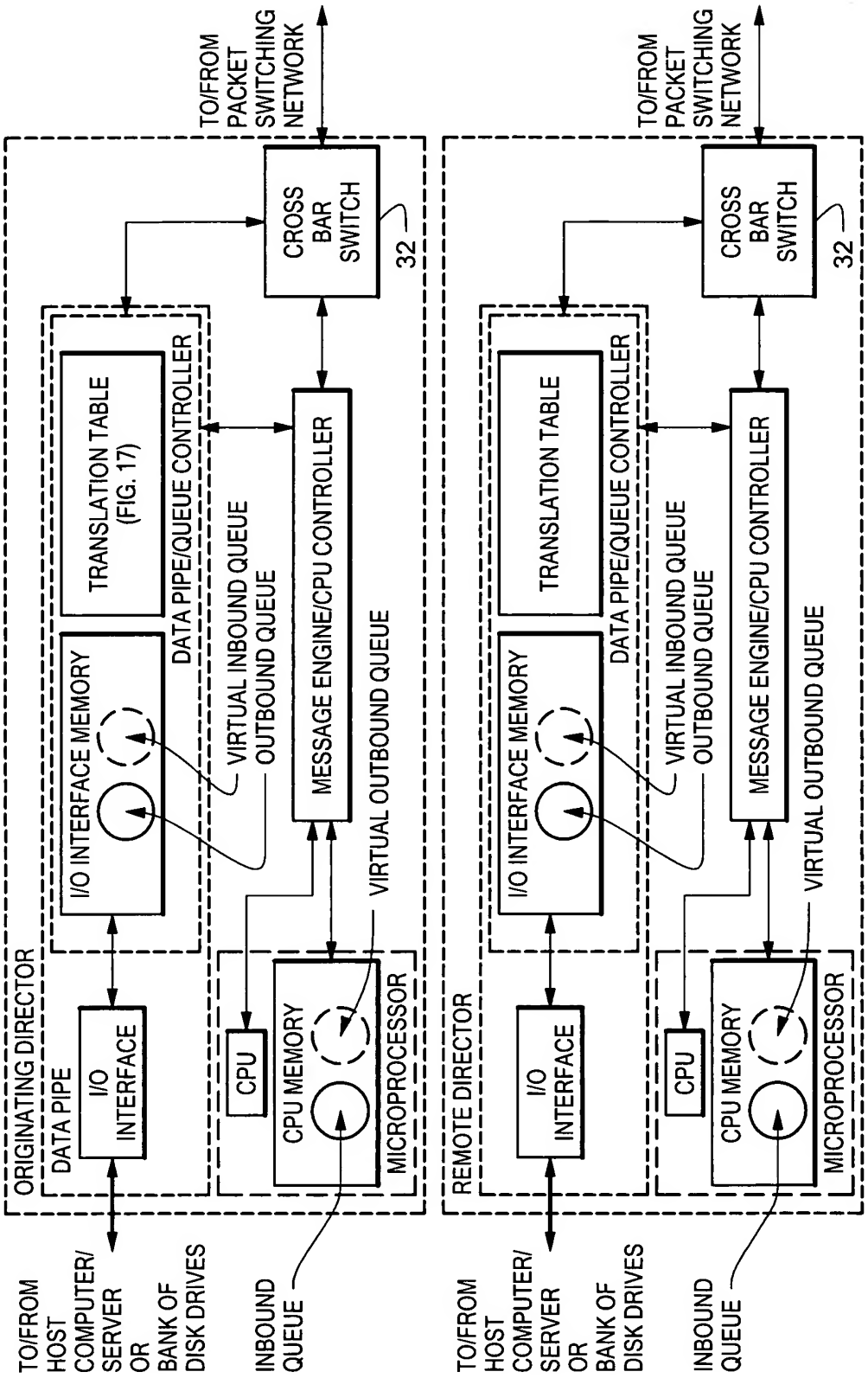
TO/FROM PACKET SWITCHING NETWORK
CROSS BAR SWITCH
32
ORIGINATING DIRECTOR
DATA PIPE
I/O INTERFACE
TRANSLATION TABLE (FIG. 17)
I/O INTERFACE MEMORY
DATA PIPE/QUEUE CONTROLLER
VIRTUAL INBOUND QUEUE
OUTBOUND QUEUE
MESSAGE ENGINE/CPU CONTROLLER
VIRTUAL OUTBOUND QUEUE
CPU
CPU MEMORY
MICROPROCESSOR
TO/FROM HOST COMPUTER/ SERVER OR BANK OF DISK DRIVES
INBOUND QUEUE
REMOTE DIRECTOR

FIG. 14

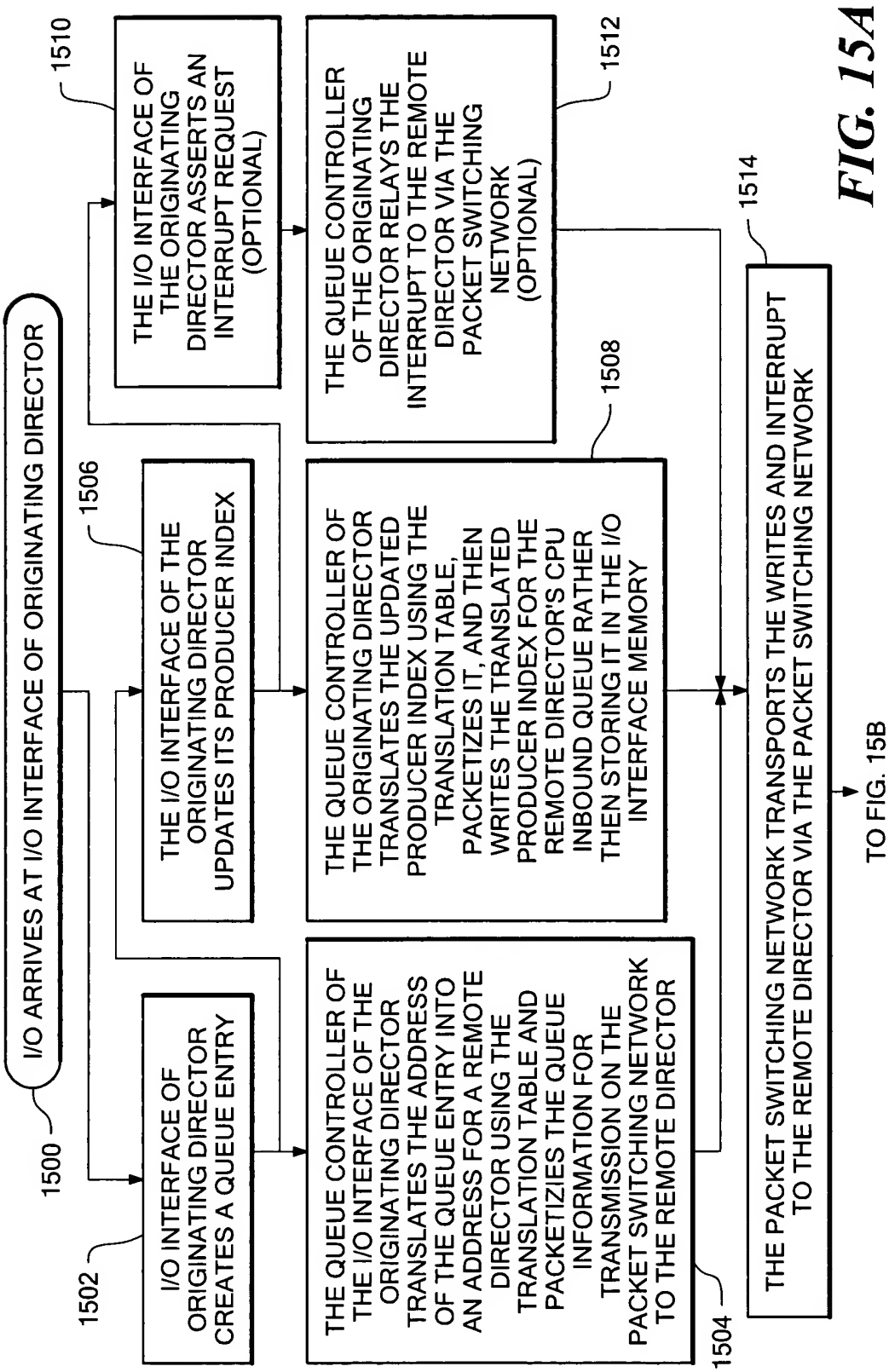
I/O ARRIVES AT I/O INTERFACE OF ORIGINATING DIRECTOR
1500
I/O INTERFACE OF ORIGINATING DIRECTOR CREATES A QUEUE ENTRY
1502
THE I/O INTERFACE OF THE ORIGINATING DIRECTOR UPDATES ITS PRODUCER INDEX
1506
THE I/O INTERFACE OF THE ORIGINATING DIRECTOR ASSERTS AN INTERRUPT REQUEST (OPTIONAL)
1510
THE QUEUE CONTROLLER OF THE I/O INTERFACE OF THE ORIGINATING DIRECTOR TRANSLATES THE ADDRESS OF THE QUEUE ENTRY INTO AN ADDRESS FOR A REMOTE DIRECTOR USING THE TRANSLATION TABLE AND PACKETIZIES THE QUEUE INFORMATION FOR TRANSMISSION ON THE PACKET SWITCHING NETWORK TO THE REMOTE DIRECTOR
1504
THE QUEUE CONTROLLER OF THE ORIGINATING DIRECTOR TRANSLATES THE UPDATED PRODUCER INDEX USING THE TRANSLATION TABLE, PACKETIZES IT, AND THEN WRITES THE TRANSLATED PRODUCER INDEX FOR THE REMOTE DIRECTOR'S CPU INBOUND QUEUE RATHER THEN STORING IT IN THE I/O INTERFACE MEMORY
1508
THE QUEUE CONTROLLER OF THE ORIGINATING DIRECTOR RELAYS THE INTERRUPT TO THE REMOTE DIRECTOR VIA THE PACKET SWITCHING NETWORK (OPTIONAL)
1512
THE PACKET SWITCHING NETWORK TRANSPORTS THE WRITES AND INTERRUPT TO THE REMOTE DIRECTOR VIA THE PACKET SWITCHING NETWORK
1514
TO FIG. 15B

FIG. 15A

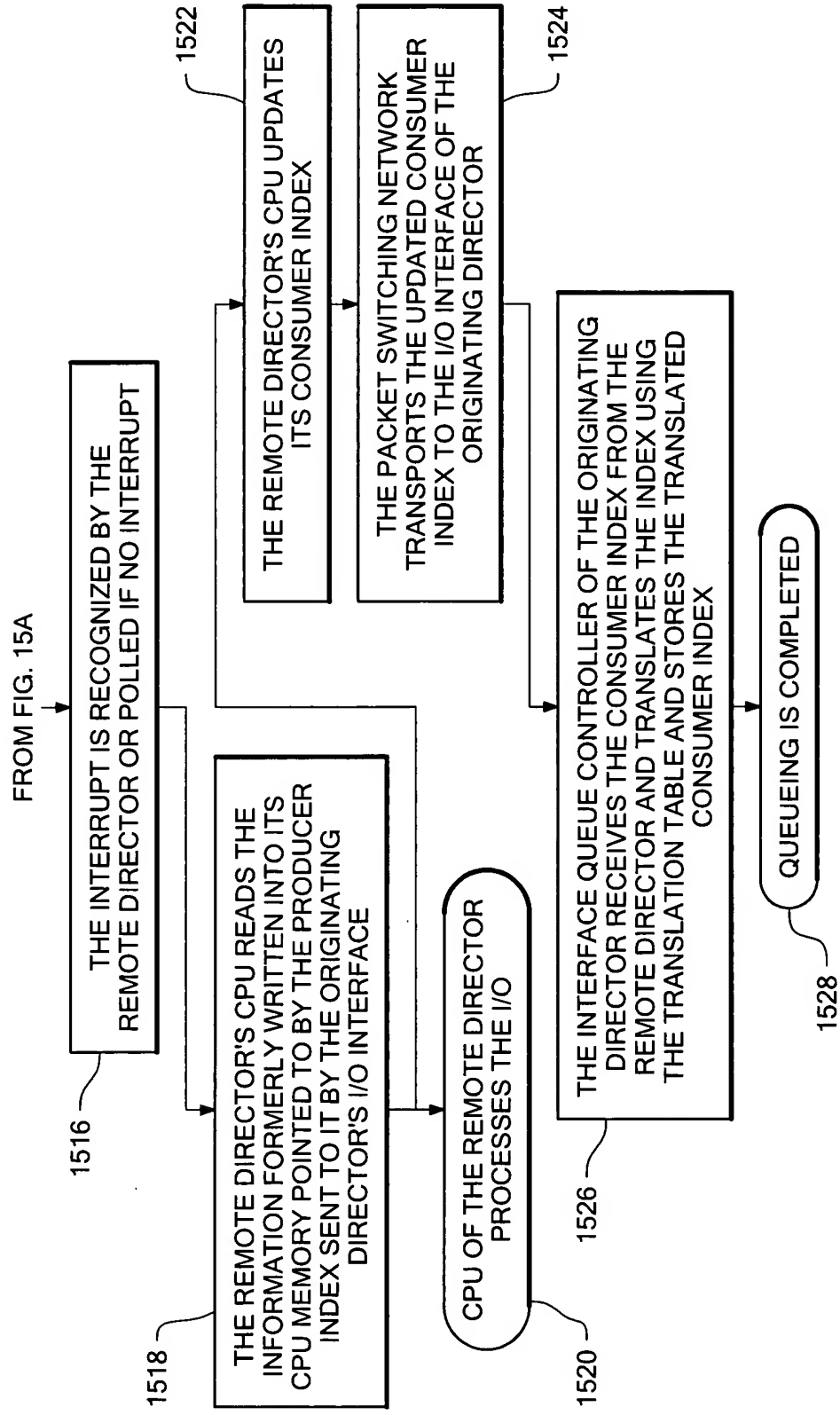
FROM FIG. 15A
THE INTERRUPT IS RECOGNIZED BY THE REMOTE DIRECTOR OR POLLED IF NO INTERRUPT
1516
THE REMOTE DIRECTOR'S CPU READS THE INFORMATION FORMERLY WRITTEN INTO ITS CPU MEMORY POINTED TO BY THE PRODUCER INDEX SENT TO IT BY THE ORIGINATING DIRECTOR'S I/O INTERFACE
1518
CPU OF THE REMOTE DIRECTOR PROCESSES THE I/O
1520
1522
THE REMOTE DIRECTOR'S CPU UPDATES ITS CONSUMER INDEX
THE PACKET SWITCHING NETWORK TRANSPORTS THE UPDATED CONSUMER INDEX TO THE I/O INTERFACE OF THE ORIGINATING DIRECTOR
1524
THE INTERFACE QUEUE CONTROLLER OF THE ORIGINATING DIRECTOR RECEIVES THE CONSUMER INDEX FROM THE REMOTE DIRECTOR AND TRANSLATES THE INDEX USING THE TRANSLATION TABLE AND STORES THE TRANSLATED CONSUMER INDEX
1526
QUEUEING IS COMPLETED
1528

FIG. 15B

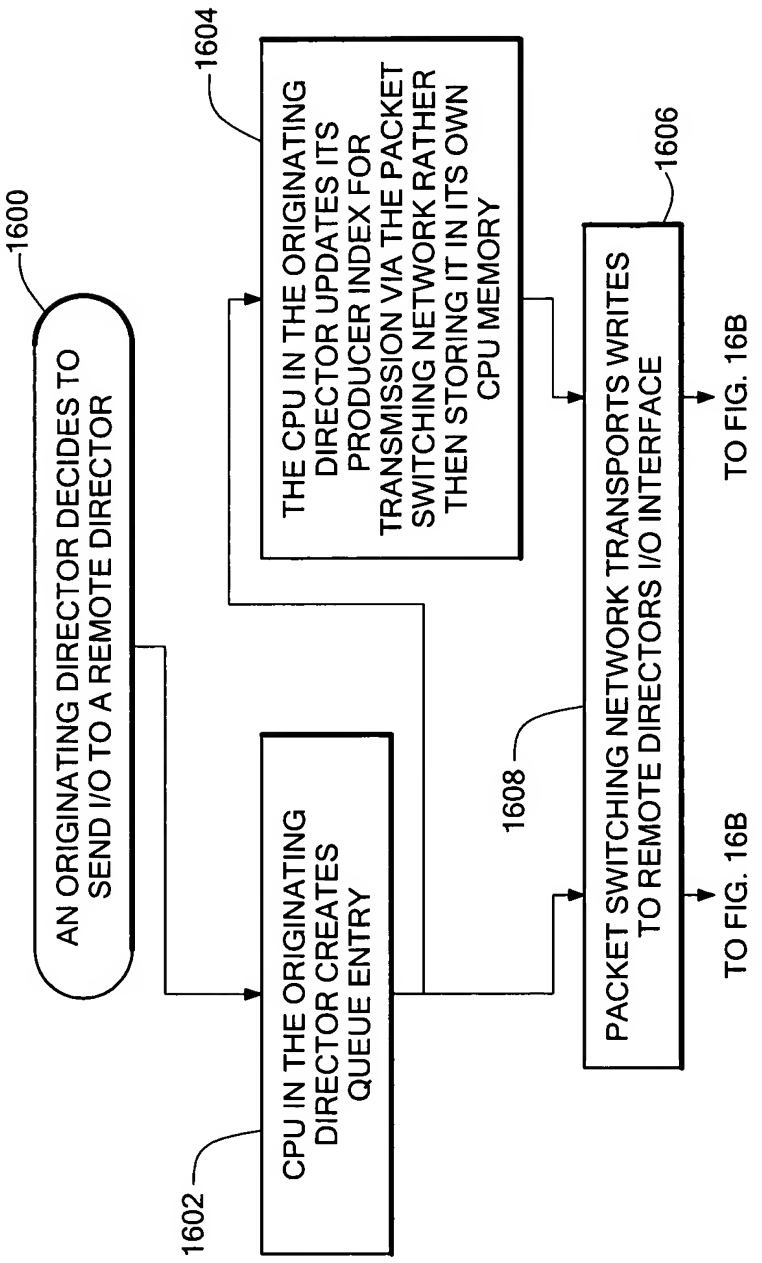
1600
AN ORIGINATING DIRECTOR DECIDES TO SEND I/O TO A REMOTE DIRECTOR
1602
CPU IN THE ORIGINATING DIRECTOR CREATES QUEUE ENTRY
1604
THE CPU IN THE ORIGINATING DIRECTOR UPDATES ITS PRODUCER INDEX FOR TRANSMISSION VIA THE PACKET SWITCHING NETWORK RATHER THEN STORING IT IN ITS OWN CPU MEMORY
1606
PACKET SWITCHING NETWORK TRANSPORTS WRITES TO REMOTE DIRECTORS I/O INTERFACE
1608
TO FIG. 16B
TO FIG. 16B

FIG. 16A

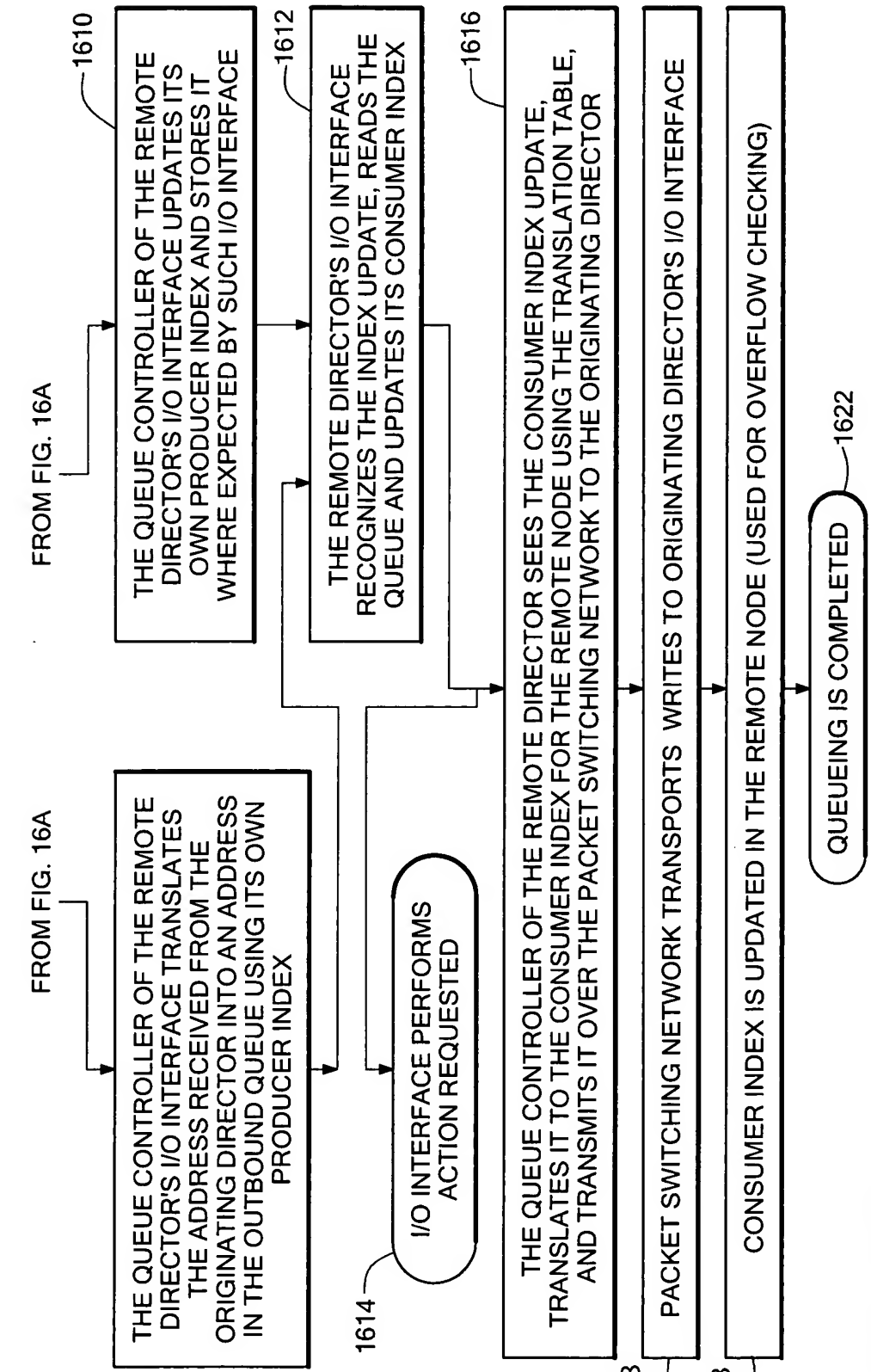
FROM FIG. 16A
FROM FIG. 16A
1610
THE QUEUE CONTROLLER OF THE REMOTE DIRECTOR'S I/O INTERFACE TRANSLATES THE ADDRESS RECEIVED FROM THE ORIGINATING DIRECTOR INTO AN ADDRESS IN THE OUTBOUND QUEUE USING ITS OWN PRODUCER INDEX
THE QUEUE CONTROLLER OF THE REMOTE DIRECTOR'S I/O INTERFACE UPDATES ITS OWN PRODUCER INDEX AND STORES IT WHERE EXPECTED BY SUCH I/O INTERFACE
1612
THE REMOTE DIRECTOR'S I/O INTERFACE RECOGNIZES THE INDEX UPDATE, READS THE QUEUE AND UPDATES ITS CONSUMER INDEX
1614
I/O INTERFACE PERFORMS ACTION REQUESTED
1616
THE QUEUE CONTROLLER OF THE REMOTE DIRECTOR SEES THE CONSUMER INDEX UPDATE, TRANSLATES IT TO THE CONSUMER INDEX FOR THE REMOTE NODE USING THE TRANSLATION TABLE, AND TRANSMITS IT OVER THE PACKET SWITCHING NETWORK TO THE ORIGINATING DIRECTOR
1618
PACKET SWITCHING NETWORK TRANSPORTS WRITES TO ORIGINATING DIRECTOR'S I/O INTERFACE
1618
CONSUMER INDEX IS UPDATED IN THE REMOTE NODE (USED FOR OVERFLOW CHECKING)
1622
QUEUEING IS COMPLETED

FIG. 16B

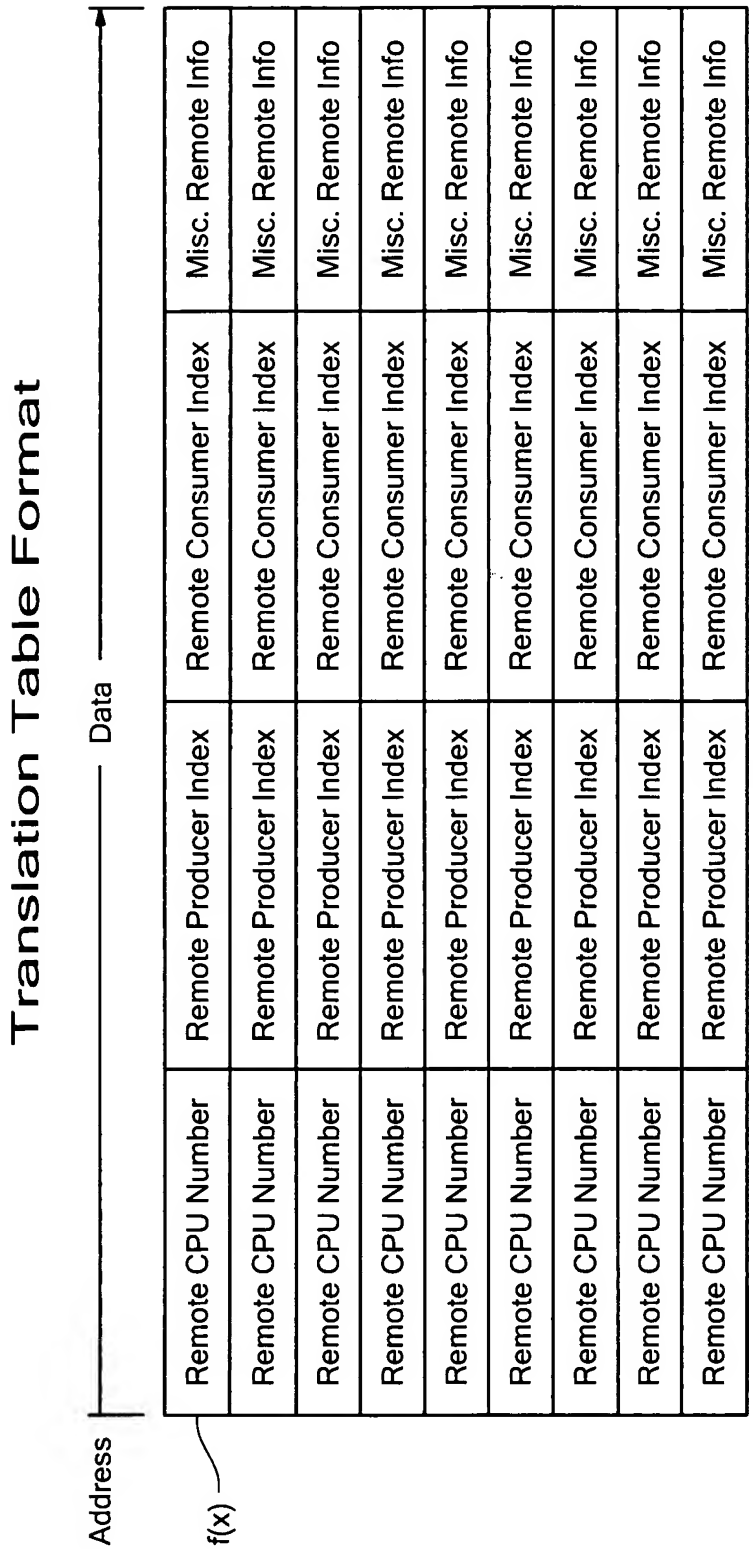
Translation Table Format
Address
Data
f(x)
Remote CPU Number
Remote Producer Index
Remote Consumer Index
Misc. Remote Info

FIG. 17